

**IN THE UNITED STATES DISTRICT COURT  
FOR THE EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION**

NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	Case No. 2:22-cv-293-JRG
vs.	)	
	)	JURY TRIAL DEMANDED
SAMSUNG ELECTRONICS CO., LTD.;	)	(Lead Case)
SAMSUNG ELECTRONICS AMERICA,	)	
INC.; SAMSUNG SEMICONDUCTOR	)	<div style="background-color: black; width: 150px; height: 1.2em;"></div>
INC.,	)	
	)	
Defendants.	)	

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NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	Case No. 2:22-cv-294-JRG
vs.	)	
	)	JURY TRIAL DEMANDED
MICRON TECHNOLOGY, INC.;	)	
MICRON SEMICONDUCTOR	)	
PRODUCTS, INC.; MICRON	)	
TECHNOLOGY TEXAS LLC,	)	
	)	
Defendants.	)	

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**NETLIST, INC.'S OPPOSITION TO MICRON'S MOTION FOR  
SUMMARY JUDGMENT OF LACK OF WRITTEN DESCRIPTION FOR  
U.S. PATENT NO. 11,093,417 (DKT. 370)**

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Micron's written description arguments gloss over or ignore expert testimony in the record that contradicts its conclusions. Micron's arguments are also contradicted by the Court's claim construction order and positions Micron has taken elsewhere in this litigation. Summary judgment is therefore inappropriate, and Micron's motion should be denied.

## **I. RESPONSE TO MICRON'S STATEMENT OF ISSUES**

A. Whether a reasonable jury could conclude that Micron has not proven by clear and convincing evidence that the '417 patent's specification lacks written description support for claim 1's "overall CAS latency" limitation.

B. Whether a reasonable jury could conclude that Micron has not proven by clear and convincing evidence that the earliest written description support for claim 1's "data buffer control signals" is found in the '417 patent's 2019 patent application.

## **II. RESPONSE TO MICRON'S STATEMENT OF UNDISPUTED FACTS**

1. Not disputed that Dr. Mangione-Smith's opening expert report was served on November 20, 2023, and includes his analysis showing why Micron's DDR4 LRDIMMs infringe the asserted claims of the '417 patent. Netlist additionally notes that Dr. Mangione-Smith's rebuttal expert report was served on December 21, 2023, and includes his rebuttal of Dr. Stone's written description arguments, which are the same as those Micron advances in its motion for summary judgment.

2. Not disputed that Micron accurately reproduced the language found in claim 1 of the '417 patent pertaining to CAS latency, i.e., the "CAS latency limitation." Micron's DDR4 LRDIMM products infringe these elements.

3. Not disputed that during the *Markman* Hearing, Netlist argued the "CAS latency" in the context of the '417 patent relates to both read and write commands. Netlist additionally argued that "the specification also makes clear that the design encompasses both read and write in dealing with latencies in the context of bo[th] read and write." Dkt. 370-03 (*Markman* transcript) at 112:6-8. And

that Micron's expert "Doctor Stone was shown the passage on CAS latency from the specification and he agreed that it could relate to both read and write transfers." *Id.* at 112:8-11.

4. Not disputed that the Court agreed with Netlist and rejected Micron's construction and alternative indefiniteness argument. Additionally noted that the Court based its agreement with Netlist that CAS latency applies to both read and write operations on the patent's pertinent disclosure, which the Court cited in full. Dkt. 228 (*Markman* order) at 33 ("Based on [’417, 22:36-61]<sup>1</sup>, the Court agrees with Netlist. The disclosure explains the one-cycle time delay 'provides sufficient time for *read and write data transfers* to provide the functions of the data path multiplexer/demultiplexer.'"). The Court also noted, *inter alia*, that "Micron's expert agrees 'CAS latency can relate to both read and write data transfers.'" *Id.* at 34 (citing Dkt. 129-5 (Stone Depo. Tr.) at 76:16–18).

5-6. Not disputed that Micron accurately reproduced the court's construction of "overall CAS latency" and "actual operational CAS latency."

7. Disputed. The Patent also discusses "overall CAS latency of the memory module" being "greater than the actual operational CAS latency of each of the memory devices" in the Abstract, and at lines 4:1-10.

8. Agreed that the exact phrase "data buffer control signals" is not used in applications prior to the '417. Disagreed that this means the concept of a data buffer control signal was not disclosed in earlier priority materials. *See* Ex. 1 (Mangione-Smith Rebuttal, Ex. B), ¶¶ 75-81. Additionally noted that the Court's *Markman* order acknowledges the term has a disclosure in the specification. Dkt. 228 (*Markman* order) at 30. Additionally noted that Dr. Stone's non-infringement argument with respect

[REDACTED]

[REDACTED] Ex. 2 (Stone Rebuttal), ¶¶ 252-53. Specifically, Dr. Stone opines that [REDACTED]

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<sup>1</sup> The Court cited and cleaned up '215, 20:22–47, which is identical to the corresponding paragraph in the '417 patent.

[REDACTED]  
[REDACTED] and that [REDACTED]  
[REDACTED]  
[REDACTED] *Id.*, ¶¶ 254-55.

### III. LEGAL STANDARD

“To satisfy the written description requirement of 35 U.S.C. § 112, ‘the disclosure of the application relied upon [must] reasonably convey[] to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.’ The written description requirement does ‘not demand any particular form of disclosure, or that the specification recite the claimed invention in haec verba.’ *Sycamore IP Holdings LLC v. AT&T Corp.*, 294 F. Supp. 3d 620, 648 (E.D. Tex. 2018) (citing *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351-52 (Fed. Cir. 2010) (en banc)). The issue of whether a claimed invention satisfies the written description requirement is a question of fact. *Centra, Inc. v. Sonitor Techs., Inc.*, 915 F.3d 1360, 1365 (Fed. Cir. 2019) (citing *Ariad*, 598 F.3d at 1351). “A party alleging that a patent is invalid for failure to comply with the written description requirement has the burden of establishing by clear and convincing evidence that the requirement was not met, in light of the presumption of validity.” *Intirtool, Ltd. v. Texar Corp.*, 369 F.3d 1289, 1294 (Fed. Cir. 2004).

“Evidence at the summary judgment stage must be viewed in the light most favorable to the non-moving party, and reasonable inferences must be drawn in that party’s favor.” *PPS Data, LLC v. Jack Henry & Assocs.*, 404 F. Supp. 3d 1021, 1037 (E.D. Tex. 2019) (citing *Fisk Elec. Co. v. DQSI, L.L.C.*, 894 F.3d 645, 650 (5th Cir. 2018)). “In a context where a party must prove its claims by clear and convincing evidence, ‘the clear-and-convincing standard of proof should be taken into account in ruling on summary judgment motions . . . .’” *Id.* at 38 (citing *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 255 (1986)).

#### IV. ARGUMENT

##### A. A Reasonable Fact Finder Can Find that the CAS Latency Limitations Have Written Description Support in the Specification

At claim construction, the Court rejected Micron's contention that the CAS latency limitation is limited to read operations. Dkt. 228 (*Markman* order) at 34 ("The Court therefore rejects Micron's position . . ."). The Court quoted the pertinent portion of the specification in full and determined that it showed that the CAS latency limitation applies to both read and write commands and crafted its construction in light of the specification's disclosure. *Id.* at 33 ("Based on this paragraph, [i.e., '417, 22:36-61,] the Court agrees with Netlist. The disclosure explains the one-cycle time delay 'provides sufficient time for *read and write data transfers* to provide the functions of the data path multiplexer/demultiplexer.' Moreover, the disclosure refers to data transfers *between* the memory controller and the memory module" rather than in only one direction or the other.") (internal citations omitted). The Court also cited Dr. Stone's deposition, wherein he admitted, "CAS latency can relate to both read and write data transfers." *Id.* at 35 (citing 2023-08-18 Stone Depo 76:16-18). Specifically, Dr. Sone admitted that the disclosure in the specification applies to both read and write operations:

Q. This passage is indicating that CAS latency can relate to both read and write data transfers?

A. That's correct.

Dkt. 129-05 at 76:16-18. Now Micron is arguing that the terms construed by the Court *in light of the disclosure in the specification* have no support in the specification. This is an internally contradictory position and is insufficient for summary judgment.<sup>2</sup> Indeed, Micron's motion for

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<sup>2</sup> Micron points out that the Court's order noted that "[w]hile it may be true, under Netlist's interpretation of 'CAS latency,' the recited limitation can never be met by an accused device, that does not mean the term is indefinite—only that infringement is impossible." Dkt 228 (*Markman* Order) at 35. These observations by the Court in no way support Micron's motion. As the Court pointed out, Micron was conflating its claim construction arguments with a potential infringement argument it could make. Likewise, Micron's reference to this discussion just highlights how it is now committing a similar error by conflating its invalidity arguments with a potential infringement argument.

summary judgment appears to be, in substance, a rehash of its indefiniteness theory, under a different paragraph of 35 U.S.C. § 112.

Beyond contradicting the court's *Markman* order, Micron glosses over the active conflict in expert testimony on the exact issue it is moving on. Micron's position in its motion mirrors the opinions of Dr. Stone in his opening report, although they do not cite his report. *See* Ex. 3 (Stone Opening Report), ¶¶ 77-83. Specifically, just as in Micron's motion, Dr. Stone argued that [REDACTED]

[REDACTED]

*Id.* ¶ 77. Dr. Mangione-Smith offered rebuttal expert testimony in his rebuttal report. Ex. 1 (Mangione-Smith Rebuttal, Ex. B), ¶¶ 82-88. Dr. Mangione-Smith explained that, for example, Dr. Stone's analysis incorrectly assumes [REDACTED]

[REDACTED] *Id.* ¶84. Dr. Mangione-Smith included diagrammatic support for his analysis:

[REDACTED]

*Id.* Dr. Mangione-Smith ties his analysis directly to the specification:

[REDACTED]

*Id.* at ¶ 85. Dr. Mangione-Smith further analyzes the specification's disclosure and concludes that:

[REDACTED]



[REDACTED]

*Id.* at ¶¶ 86-87. Tellingly, while Micron moved to strike various opinions in Dr. Mangione-Smith’s reports, including portions of his infringement analysis related to the CAS latency limitation, Micron did not move to strike the above opinions on written description. *See* Dkt 369. Here, however, Micron argues in conclusory fashion that Dr. Mangione-Smith is engaging in “improper and untimely claim construction” because, for write operations, he [REDACTED]

[REDACTED] This is a proper application of the court’s construction to the technology in question in light of the specification. Micron and its expert may disagree with this and other opinions of Dr. Mangione-Smith, but that simply creates a classic battle of the experts regarding § 112 that is not amenable to summary judgment. *ROY-G-BIV Corp. v. ABB, Ltd.*, 63 F. Supp. 3d 690, 697 (E.D. Tex. 2014) (“Whether the . . . disclosures adequately describe a system that meets the limitations of the claims is a question of fact. That each party’s expert comes to a different conclusion on this issue demonstrates that genuine issues of material fact remain that preclude summary judgment.”) (citing *Butamax Advanced Biofuels LLC v. Gevo, Inc.*, 746 F.3d 1302, 1316 (Fed. Cir. 2014)).

Other evidence also undermines Micron’s position. For example, in the ’417 patent’s Notice of Allowance, the examiner specifically noted that the CAS latency limitation was “*taught by the specification as originally filed.*” Ex. 4 at NL-MS-293 00008342 (emphasis added).

**B. A Reasonable Fact Finder Can Find that the Concept of “data buffer control signals” Has Written Description Support Predating the ’417 Patent Application**

Micron asks the Court to find, as a matter of law, that the ’417 patent “introduces the concept of ‘data buffer control signals’ for the first time in the application for the ’417 patent filed in November

25, 2019” because the ’417 patent uses the phrase “data buffer control signal” in its Abstract and Summary of Invention where prior applications in the chain used the phrase “control signal” but not “data buffer control signal.” Mot. at 8-9. Micron’s request should be denied. The ’417 patent issued from a continuation application claiming priority to a series of prior applications going back to 2004. *See* Ex. 5 (’417 patent), at 1-2 (noting Related U.S. Application Data). During prosecution, the examiner concluded that the “data buffer control signal” limitation was “taught by the specification as originally filed” and “not taught or suggested by the prior art of record,” identifying the “closest prior art” as a patent publication from 2003 (“Janzen”) but noting that it failed to teach the data buffer control signal limitation. *See* Ex. 4 (’417 Notice of Allowance) at NL-MS-293\_00008342-NL-MS-293\_00008343. Micron itself conceded, in its claim construction brief, that “support for [the data buffer control signals] term is found in the original specification’s disclosure of ‘control signals,’” even though the phrase “data buffer control signal” did not literally appear in the priority document. Dkt. 143 (Defendants’ Claim Construction Br.) at 19.

Micron’s rebuttal expert report on infringement also contradicts its position here. Its expert, Dr. Stone, opines that a person of ordinary skill would understand [REDACTED] [REDACTED] *see* Ex. 2 (Stone Rebuttal), ¶ 255, which is described in applications predating 2019, e.g., in the parent application filed in 2017 that issued as the ’314 patent. *See* Ex. 6 (U.S. Patent No. 10,489,314) at Abstract (“The logic is configured to respond to a first memory command by providing first control signals to the data buffer to enable communication of at least one first data signal between the first memory integrated circuits and the memory controller through the data buffer, and is further configured to respond to a second memory command by providing second control signals to the data buffer to enable communication of at least one second data signal between the second memory integrated circuit and the memory controller through the data buffer.”), 7:20-23 (“In certain embodiments, the circuit 40 further comprises one or more switches which are operatively

coupled to the logic element to receive control signals from the logic element.”).

Indeed, even in his opening report on invalidity, Dr. Stone [REDACTED] Ex. 3 (Stone Opening), ¶ 71. Dr. Stone only contends that [REDACTED] [REDACTED] [REDACTED] [REDACTED] *Id.*, ¶ 74. But as explained in Dr. Mangione-Smith’s rebuttal report, [REDACTED] [REDACTED] [REDACTED] [REDACTED] noted by Dr. Stone; for example, [REDACTED] [REDACTED] which [REDACTED] [REDACTED] as well as [REDACTED] [REDACTED] Ex. 1 (Mangione-Smith Rebuttal, Ex. B), ¶ 77. [REDACTED] [REDACTED] [REDACTED]. *Id.*, ¶¶ 78-80 (noting [REDACTED] and [REDACTED] and [REDACTED] control signals). He also notes that in another exemplary embodiment, labeled [REDACTED] [REDACTED] [REDACTED] which as noted in Verilog Example 1 [REDACTED] [REDACTED] *Id.*, ¶ 81. All of the disclosures identified by Dr. Mangione-Smith as supporting the “data buffer control signals” limitation are present in the predecessor applications to which the ’417 patent claims priority, creating at least a triable issue of fact regarding Micron’s assertion that the ’417 patent claims are not entitled to their claimed priority date.<sup>3</sup> See *ROY-G-BIV Corp. v. ABB, Ltd.*, 63 F. Supp. 3d 690, 697 (E.D. Tex. 2014).

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<sup>3</sup> Notably, despite moving to strike various of Dr. Mangione-Smith’s opinions, Micron did not raise any objection to his responsive analysis on written description for “data buffer control signals” in the pre-2019 specification. See Dkt 369

## V. CONCLUSION

For the foregoing reasons, Netlist respectfully requests Micron's motion be denied.

Dated: January 30, 2024

Respectfully submitted,

/s/ Jason G. Sheasby

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**CERTIFICATE OF SERVICE**

I hereby certify that, on January 30, 2024, a copy of the foregoing was served to all counsel of record.

/s/ Yanan Zhao  
Yanan Zhao

**CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL**

I hereby certify that the foregoing document and exhibits attached hereto are authorized to be filed under seal pursuant to the Protective Order entered in this Case.

/s/ Yanan Zhao  
Yanan Zhao